ABSTRACT

A state machine implemented controller is provided in which a logic core 20 is reconfigurable in response to state data held within a memory 22. Thus, on transition from one state to a next state the data held within the memory 22 is used to reconfigure the operation of the logic core 20. This enables a relatively compact logic core 20 to be used time and time again, thereby avoiding the need to individually define a logic core appropriate to each individual one of the states that the state machine can enter into. This results in a controller which is much more compact on an integrated circuit die than is the case with prior art controllers.